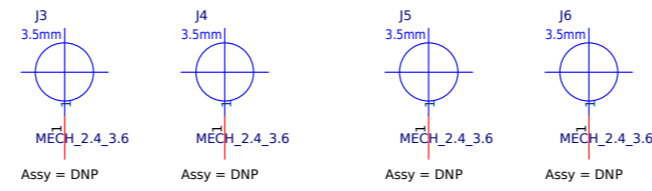
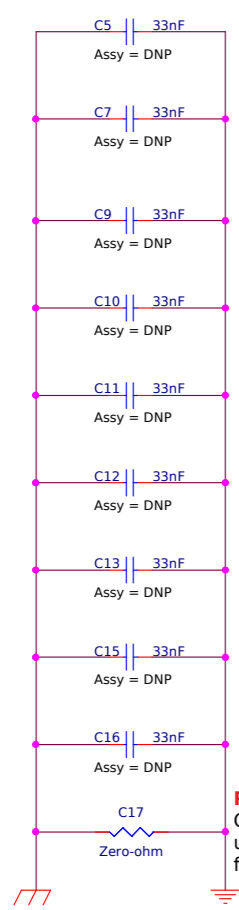


Four mechanical holes for the MicroSoM

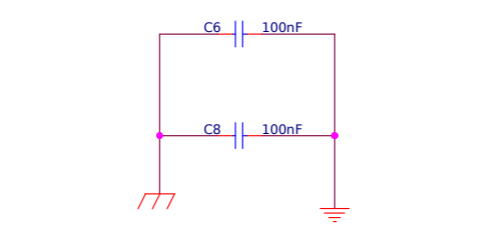


Bypass capacitors between GNDC and GND

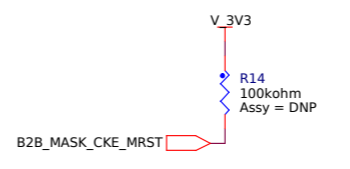
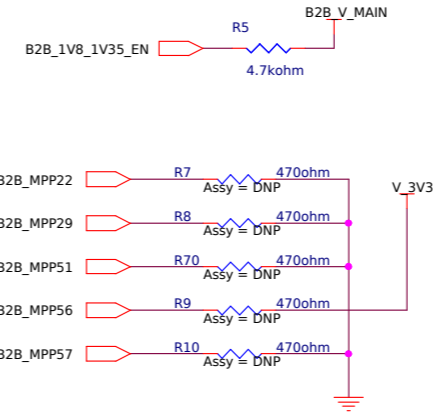
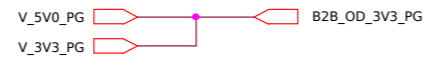


Post-production rework: Populating C17 with a Zero Ohm resistor in order to re-connect GNDC to GND to fix USD card detect pin issue created by the change of R17 from Zero Ohm to 1Meg in Rev 1.2

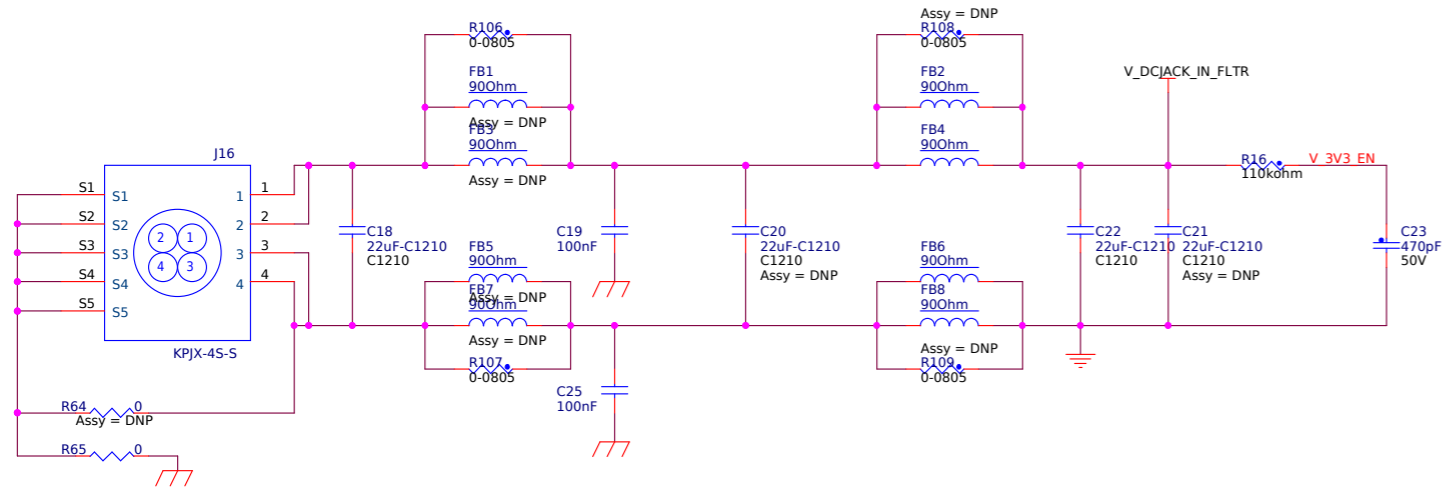
Bypass capacitors for MDIO passing underneath GNDC



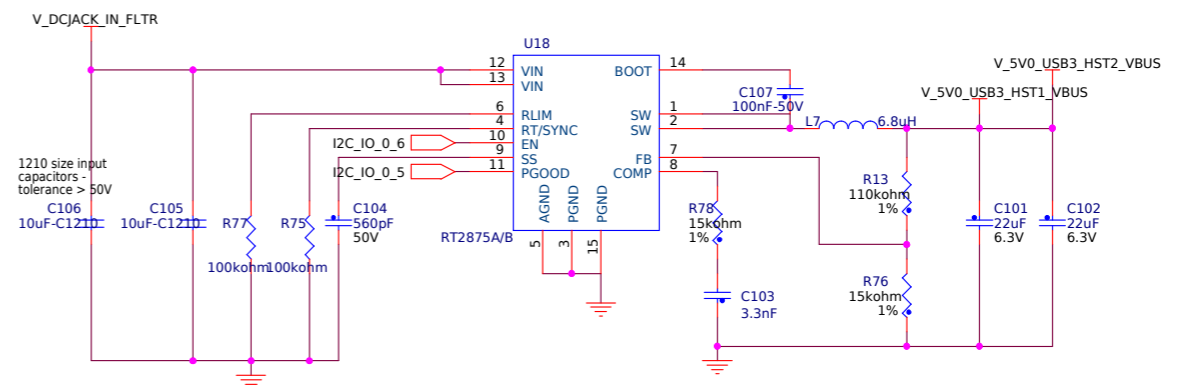
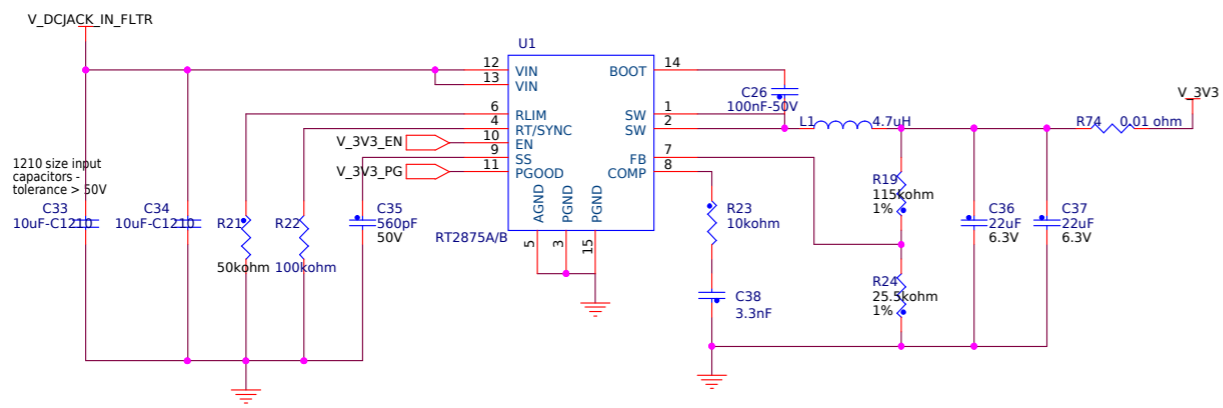
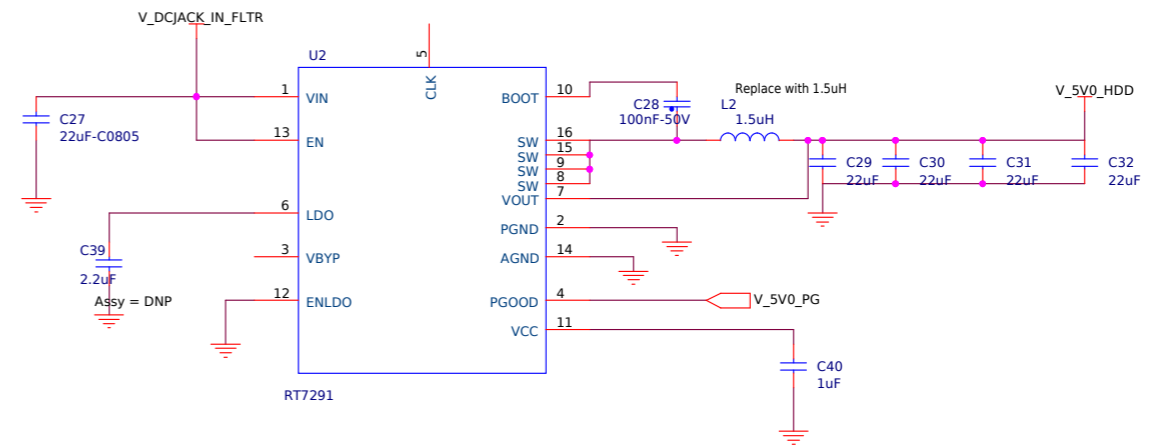
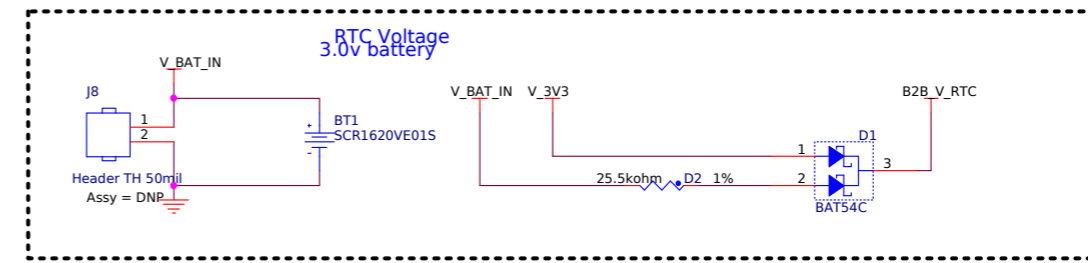
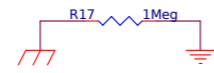
Carrier DC-DC PGOOD Signals will enable CPU DC-DC on uSoM. Signal is pulled up on uSoM.



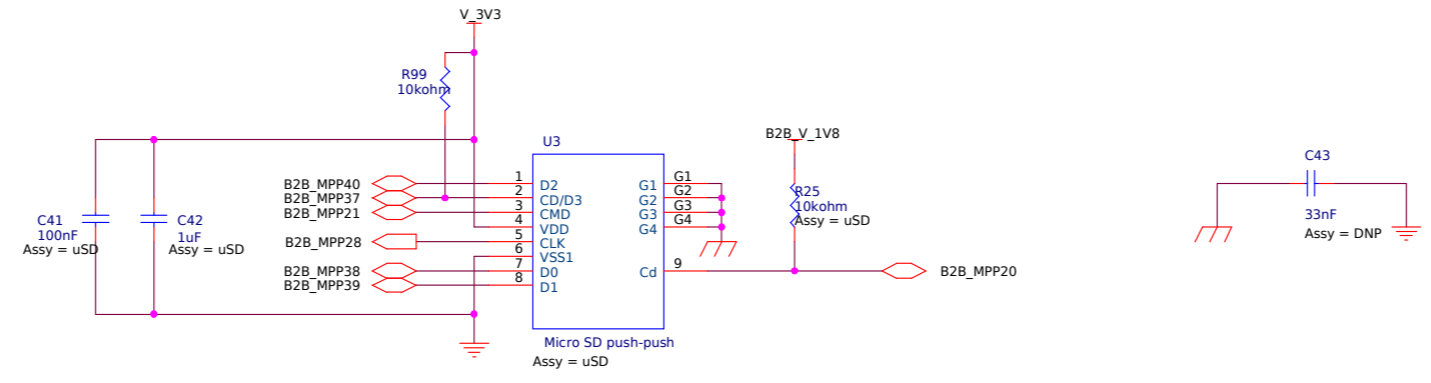
Power Jack



Prevent GND and GNDC DC biasing

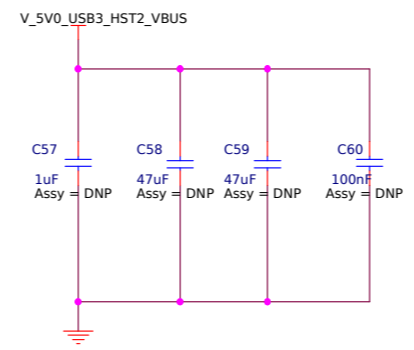
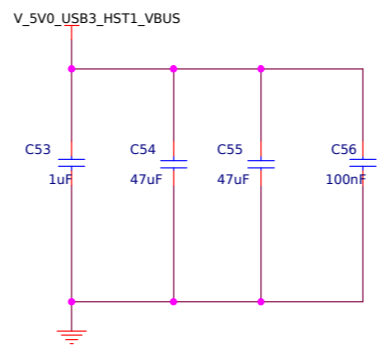
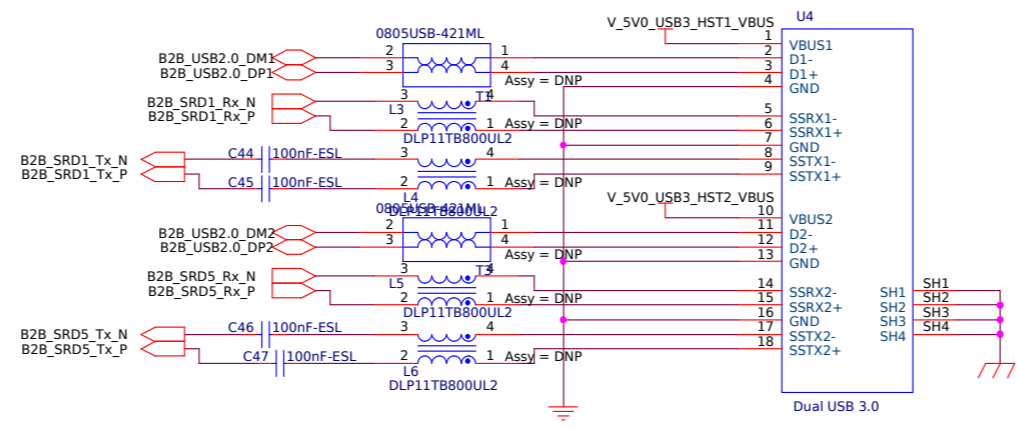


uSD

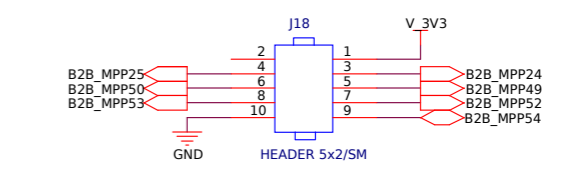
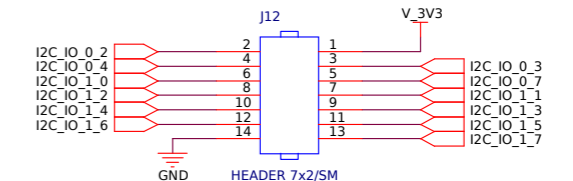
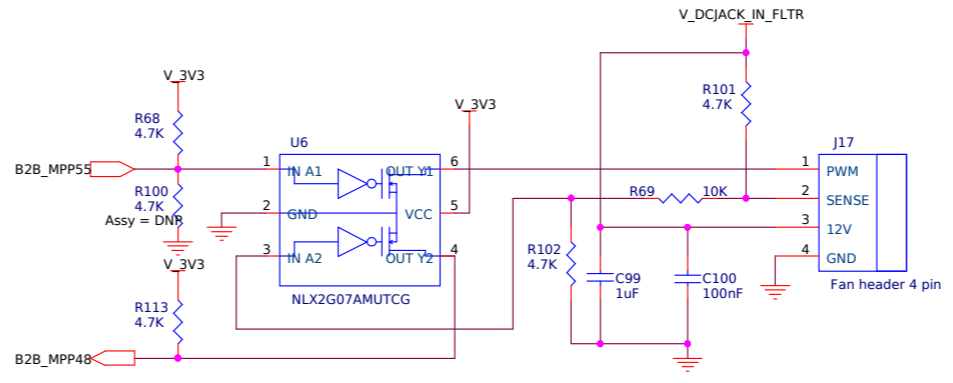
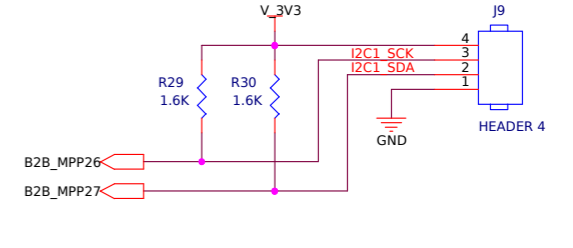
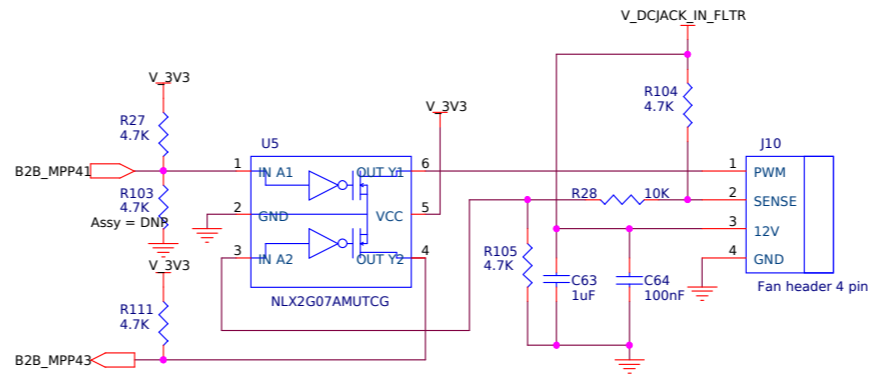
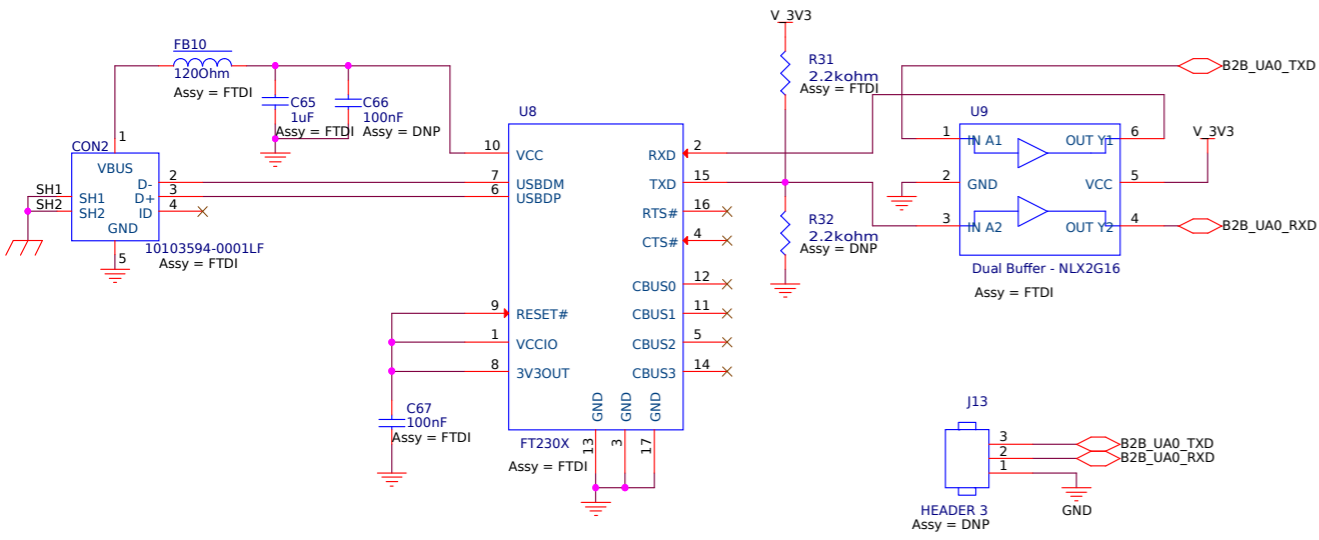


Dual USB-3 Type A

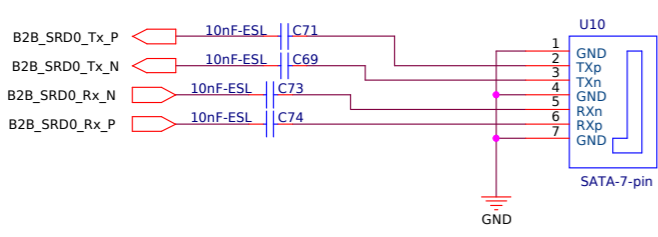
- R81 ~~~~~ 0
- R82 ~~~~~ 0
- R83 ~~~~~ 0
- R84 ~~~~~ 0
- R85 ~~~~~ 0
- R86 ~~~~~ 0
- R87 ~~~~~ 0
- R88 ~~~~~ 0
- R89 ~~~~~ 0
- R90 ~~~~~ 0
- R91 ~~~~~ 0
- R92 ~~~~~ 0



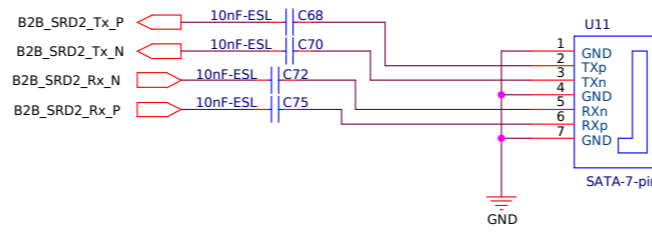
microUSB to UART



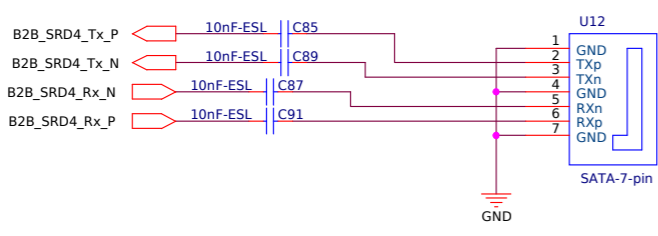
SATA0



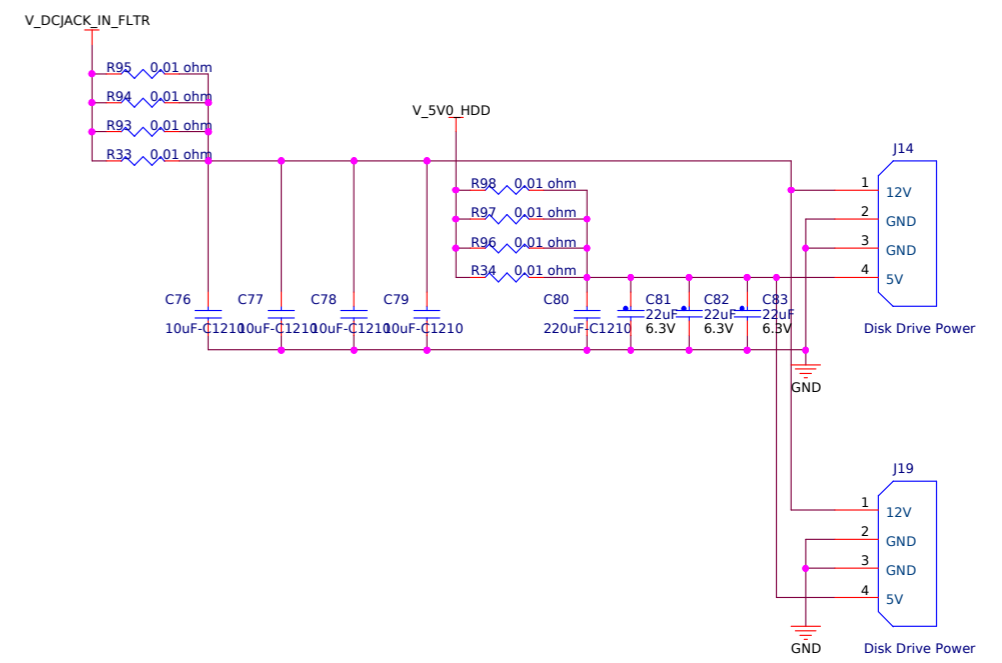
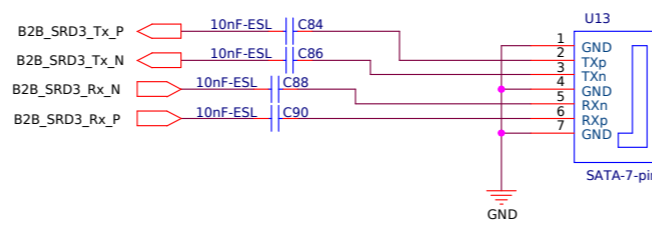
SATA1

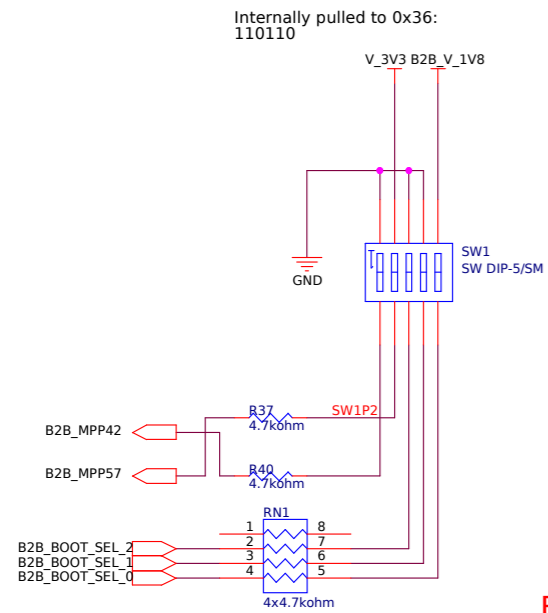


SATA2

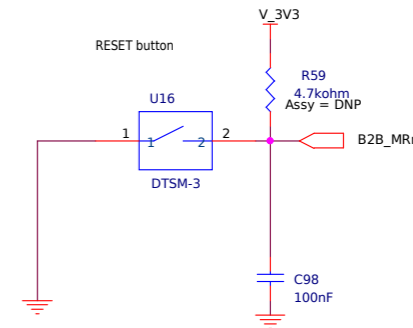
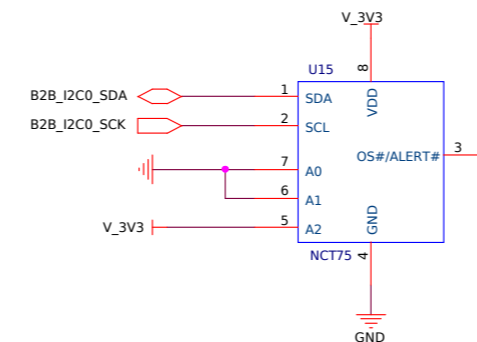
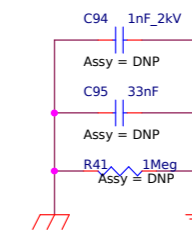
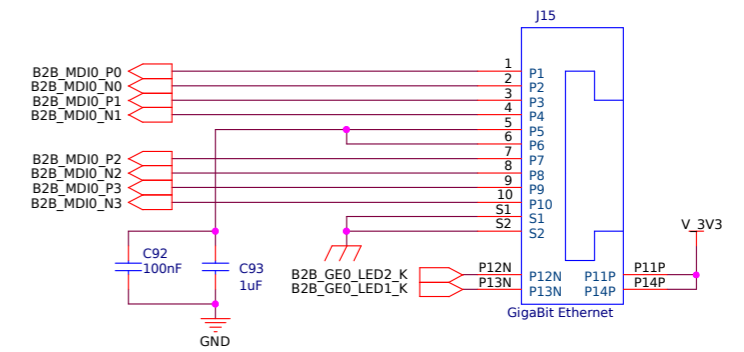
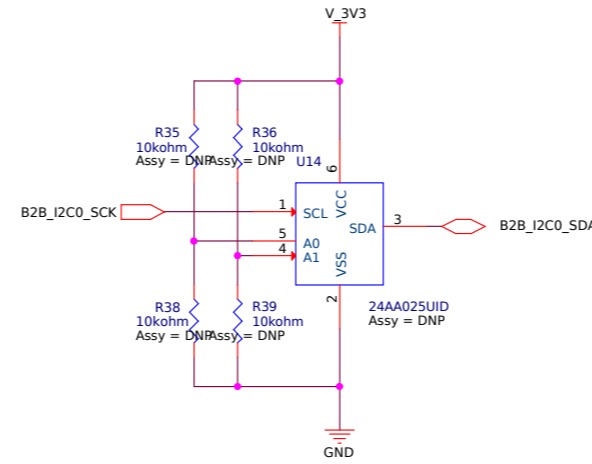
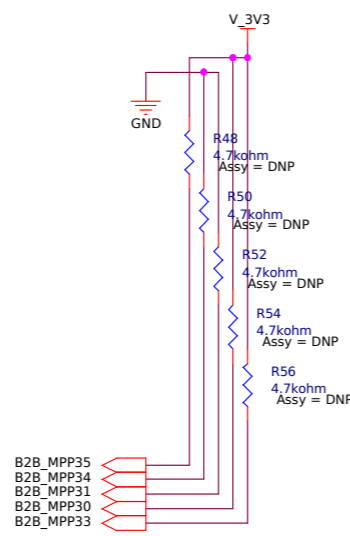
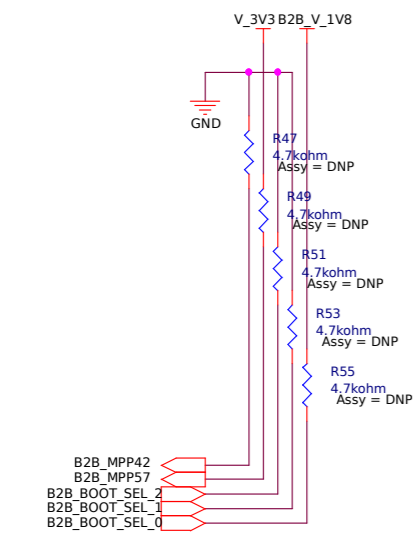


SATA3



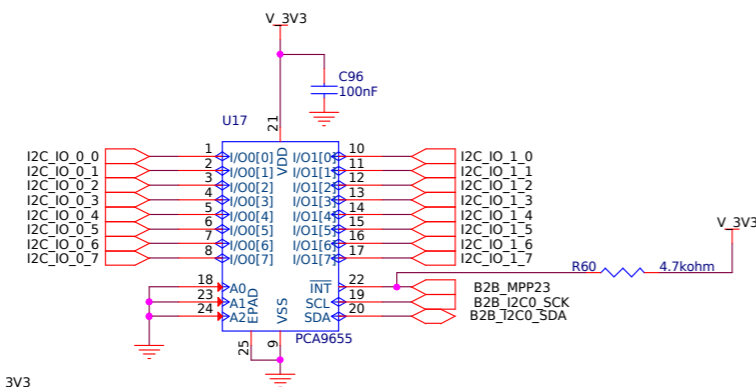


Frequency default Assy



I2C Add: 0x21 I/O Table

I02_0	I02_1	I02_2	I02_3	I02_4	I02_5	I02_6	I02_7	I03_0	I03_1	I03_2	I03_3	I03_4	I03_5	I03_6	I03_7
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Board revision.

